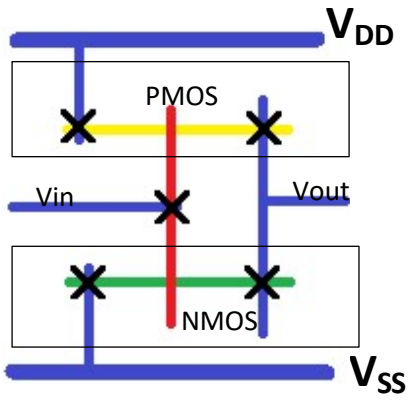
Layout of an inverter: from Stick Diagram to physical layer

One way to look at the physical layout of systems at a rather high level is with a stick diagram representation. A stick diagram of an inverter is shown below with:

- Blue Lines – Metal 1
- Yellow Lines – P-diffusion, which is an N-well, P-select, and P-active
- Green Lines – N-diffusion, made of N-select and N-active
- Red Lines – Polysilicon
- Black X – Connection (Via)

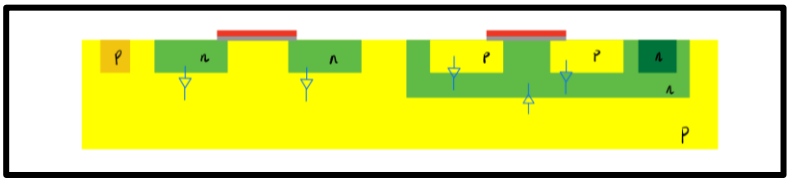


Layout the inverter by creating an n-channel and a p-channel transistor and the necessary connections to make your design look like the stick diagram. You already created a p-channel device in the previous laboratory experiment so you will need to add the n-channel transistor as well as the Metal 1 bus on top for V_{DD} and on the bottom for V_{SS}. You will also need to actually connect the drains and sources of the n-channel and p-channel devices with vias and Metal 1, but we will do that in the next few steps.

Bulk Connections

We generally look at n-channel and p-channel devices as if they are three-terminal components, being made of only a gate, drain, and source. In reality, MOSFETs have four terminals, with the fourth being the "bulk." In Virtuoso, the bulk connection for the nmos4 or pmos4 is the terminal located between the drain and source.

The bulk connection serves several purposes in the operation of a MOSFET, including having an effect on the device's threshold voltage, but we'll ignore those purposes for this lab. What is important to realize right now is that, when you manufacture a MOSFET, you create a number of PN Junctions throughout the body of the device. Recall that a PN Junction forms a diode, as shown in the image below:



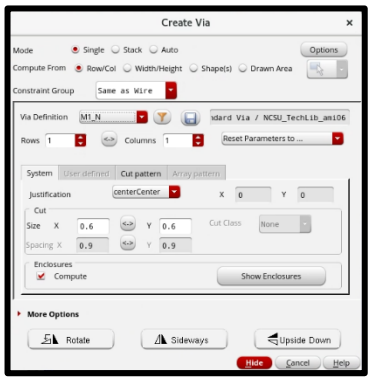
While these parasitic diodes can be useful in some cases (in fact, many cases), they can also be harmful. Consider if one of these diodes somehow becomes forward biased. Because the resistance that they see in series with them is minimal, if a single diode becomes forward biased, it can begin conducing large amounts of current – ultimately, enough current to destroy the MOS device that it is inside of. For this reason, it is critical that these parasitic diodes are kept reverse biased. This is one of the purposes of the MOSFET's bulk connection. In the image above, the extra p-doped region to the left of the n-channel device and the n-doped region to the right of the p-channel device form the bulk connections. In an n-channel device, the bulk connects to the p-substrate, and so it is desirable for this bulk to be connected to the lowest voltage present in a circuit (that is, V_{SS}). Because the n-channel bulk connects to the p-substrate, and there is only one p-substrate in an IC with the bulk CMOS process we are working with, it is only technically necessary to have one NMOS bulk connection in the circuit layout. In a p-channel device, the bulk connects to the n-well, and so it is often desirable for this bulk to be connected to the highest voltage present in the circuit (V_{DD}). Because the p-channel bulk connects to an n-well surrounding the p-channel device, it is necessary for every p-channel device in the layout to have its own bulk connection if there the n-wells for each p-channel device are electrically isolated from each other. It is possible to put several p-channel devices in a single n-well and in this case a single bulk connection for several p-channel devices is possible.

The **most common thing for new students to forget** when designing the layout is to create bulk connections. As stated in the previous paragraph, **each p-active region requires a bulk connection**. For the p-channel device, a via called an "NTap" is used to form the bulk connection. The n-active regions also need a bulk, so for these we will use the "M1_P" via. Unlike the NTap, most designs we will be making will only need one M1_P connection for the entire design.

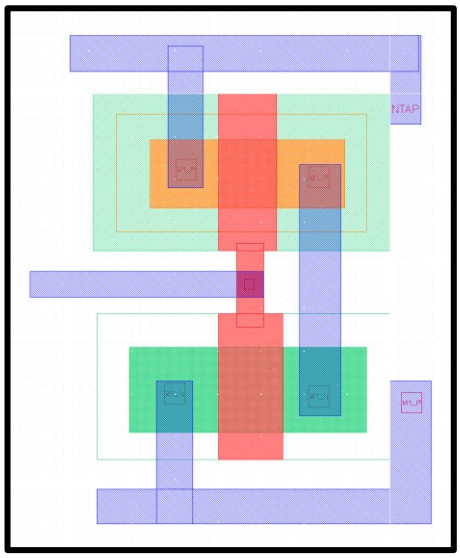
For reasons that will be discussed later, however, it is common to have more than one connection to an n-well or a p-bulk and these connections must be strategically placed. This is necessary to prevent an undesired phenomenon that can cause the circuit to fail during normal operation that is termed "latchup". At this point, we will not worry about latchup issues.

After setting the NMOS bulk, we now need to address the Drain and Source connections to both the NMOS and PMOS. These connections need to be made to the P-active and N-active regions. Use an M1_P and M1_N for P active and N active respectively, and then use Metal 1 rectangles to route the connection where you need it.

Now the only connection left is for the gates of the MOS devices, which are already made of POLY. For routing purposes, you can use "M1_Poly" to go from the Poly layer to Metal 1.



Your layout should now look something like this:



Invertor for reference

Pins

The final step to complete your layout will be to make inputs and outputs for your circuit. This is done so that when you use your component's layout in other designs, you will be able to run a check to make sure everything is connected to the right ports.

To create a pin, go to **Create → Pin**. Make sure the pins are consistent with the schematic: names *and* I/O types. **Pin names** are **case sensitive** and **cannot be changed** without deleting and remaking them. Any other variables of a pin, such as its layer or I/O type can be changed in its properties later. Check the **Display Terminal Name (now called Create Label)** and **Physical Only** boxes. When you know where the pin goes, make sure to have the same layer selected in the Layers toolbox.

Create the pins for your Input, Output, and V_{SS} and V_{DD}. Once complete, run a DRC on your circuit. The CIW output showing a DRC with zero errors is your first checkpoint for this lab.

Keyboard Shortcuts

When placing features and editing, use of the GUI in the layout editor can be a slow tedious process. There are some keyboard shortcuts that can speed up this process. Some are summarized in this section.

Useful keyboard shortcuts in schematic view:

Action	Key
Add Instance	i
Add Pin	P
Wire	w
Undo	u
Redo	shift +u
Properties	q
Rotate	r
Copy	c
Check and Save	F8
Zoom to Fit	f
Move	m
Wire Name	L

Useful keyboard shortcuts in layout view:

Action	Key
Create rectangle	r
More detail in layout	shift + f
Less detail in layout	ctrl + f
Stretch rectangle	s
Zoom to Fit	f
create ruler	k
clear all rulers	shift + k
Undo	u
Redo	shift +u
Copy	c
Properties	q